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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,963	03/30/2004	Mitsuo Kawaji	2004_0491A	2886

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EXAMINER	
MILLER, PATRICK L	

ART UNIT	PAPER NUMBER
2837	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,963	KAWAJI ET AL.	
	Examiner	Art Unit	
	Patrick Miller	2837	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-10* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03302004;06252004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Figures 11-14 are labeled "Prior Art." Therefore, the specification, under "Brief Description of the Drawings," needs to explicitly state that these figures are Prior Art. Appropriate correction is required.

Claim Objections

2. Claims 1-10 are objected to because of the following informalities: see bullet(s) below. Appropriate correction is required.

   - Claims 1 and 10 recite the acronym "PN." Because it is not immediately apparent what PN is, at the first occurrence, define the term with the acronym in parenthesis "()."

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 2, 6, 7, and 10 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 10, and 11 of copending Application No. 10/807,231. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following:

   - With respect to claims 1 and 2 and 10 of the present application and claims 1 and 11 of the copending application, the limitations of claims 1 and 2 are encompassed by claim 1 of the copending application, and the limitations of claim 10 is encompassed by claim 11 of the copending application. Also note that the term "ratio" found in claims 1 and 10 of the present application and "comparing" found in claims 1 and 11 of the copending application are interpreted as the same since a ratio is a comparison.
   - Claim 6 of the present application is not patentably distinct from claim 9 of the copending application.
   - Claim 7 of the present application is not patentably distinct from claim 10 of the copending application.
   - This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. Claims 1 and 10 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 4 of copending Application No. 10/827,289 in view of Kumaki (4,992,718).

   - The only significant difference between the claims of the present application and the claims of the copending application is that the copending claims recite an

overvoltage protection circuit. Kumaki discloses an overvoltage detecting circuit that is connected between the DC buses of an inverter and is in parallel with a capacitor (Fig. 2, #15). The motivation to use an overvoltage protector is to prevent the inverter and motor from being damaged by excessively high bus voltage (cols. 5/6, ll. 49-68/1-15). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the limitations of claims of the present invention, an overvoltage detecting circuit which provides the advantage of preventing the inverter and motor from being damaged due to excessive DC bus voltage, as taught by Kumaki.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaji et al (WO 03/081765).

- With respect to claims 1 and 10, Kawaji et al disclose an inverter controller for a motor, comprising: an AC power supply (Fig. 21, #1); a rectifier formed of a diode bridge (Fig. 21, #2); an inverter for driving a compressor (Fig. 21, #3; see also Figs. 6 and 8 (depicting outputs for compressors)); a capacitor connected between DC bus lines of the inverter (Fig. 21, capacitor between #s 2 and 3); a motor voltage command generator that generates a voltage command value based

on an external speed command (Fig. 21, #17 based on input to #14, ω*); a PN voltage detector that detects a DC voltage value (Fig. 21, #33); a PN voltage corrector that calculates a ratio of the DC voltage detection value and a DC voltage reference value to generate a PN voltage correction factor (Fig. 21, #31; see also p. 27, ll. 3-25; equation 42); and a motor voltage command corrector that generates a motor voltage command correction value (Fig. 21, #35).

- Kawaji et al do not disclose a reactor connected to the rectifier.
- With respect to the reactor, the Examiner takes Official Notice. The reason to implement a reactor into the device of Kawaji et al is to smooth out the DC current flowing in the link, and to limit the rate of rise of current should a fault occur. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the device of Kawaji et al a reactor, thereby providing the advantages of smoothing the DC current and limiting the rate of rise of current, respectively.
- With respect to claim 5, the PN voltage corrector increases the PN voltage correction factor in proportion to the DC voltage detection value when the DC voltage detection value is larger than the DC voltage reference value (col. 18, l. 10; equation 42, σRh increases when V0 is greater than Vdc).

6. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (5,206,575) in view of Morimoto et al (JP 11-308894 A).

- With respect to claims 1 and 10, Nakamura et al disclose an inverter controller with a rectifier connected to an AC power source (Fig. 1, #23), the rectifier including a diode bridge (Fig. 1, #24); an inverter that drives a compressor (Fig. 1,

#29; see also col. 1, ll. 10-12; where brushless and inductions motors are known to driver compressors); a capacitor connected between the DC bus lines (Fig. 1, #26); a voltage command generator that generates a voltage command value based on the motor speed command (Fig. 2, output of #41 based on ω^*); and a motor voltage command corrector which generates a motor voltage command correction value (Fig. 2, output of #43).

- Nakamura et al do not disclose a reactor connected to the rectifier, a PN voltage detector, and a PN voltage corrector.
- With respect to the reactor, the Examiner takes Official Notice. The reason to implement a reactor into the device of Nakamura et al is to smooth out the DC current flowing in the link, and to limit the rate of rise of current should a fault occur. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the device of Nakamura et al a reactor, thereby providing the advantages of smoothing the DC current and limiting the rate of rise of current, respectively.
- Morimoto et al disclose a PN detector that detects a DC voltage value of the inverter (Fig. 1, #4); and a PN voltage corrector which calculates a ratio of the DC voltage detection value and a predetermined DC reference value to generate a PN voltage correction factor (Abstract, "Solution" where when the device compares the DC value to Vu2 is interpreted to be analogous to a ratio and a correction factor is sent to Fig. 1, #5 to either reduce the motor's rotating speed). The motivation to use a PN detector and corrector as described is to extend the time required until control is disabled during power failure (Abstract).

- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the device of Nakamura et al a PN detector and corrector, respectively, that provides the advantage of extending the time required until control is disabled during power failure, as taught by Morimoto et al.

7. Claims 1, 4, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al (5,206,575) in view of Gilbreth et al (6,489,692).

- With respect to claims 1 and 10, Nakamura et al disclose an inverter controller with a rectifier connected to an AC power source (Fig. 1, #23), the rectifier including a diode bridge (Fig. 1, #24); an inverter that drives a compressor (Fig. 1, #29; see also col. 1, ll. 10-12; where brushless and inductions motors are known to driver compressors); a capacitor connected between the DC bus lines (Fig. 1, #26); a voltage command generator that generates a voltage command value based on the motor speed command (Fig. 2, output of #41 based on ω^*); and a motor voltage command corrector which generates a motor voltage command correction value (Fig. 2, output of #43).
- Nakamura et al do not disclose a reactor connected to the rectifier, a PN voltage detector, and a PN voltage corrector.
- With respect to the reactor, the Examiner takes Official Notice. The reason to implement a reactor into the device of Nakamura et al is to smooth out the DC current flowing in the link, and to limit the rate of rise of current should a fault occur. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the device of Nakamura et al a

reactor, thereby providing the advantages of smoothing the DC current and limiting the rate of rise of current, respectively.

- Gilbreth et al disclose a PN detector that detects a DC voltage value of the inverter (Fig. 3, #20); and a PN voltage corrector that calculates a ratio of the DC voltage detection value and a predetermined DC reference value to generate a PN voltage correction factor (Fig. 3, #214 calculates the correction factor based on #212 and #216, where the comparator provides a signal analogous to a ratio; see also col. 7, ll. 50-64). The motivation to use a PN detector, corrector, and associated circuitry is to provide the advantage of regulating the voltage applied to a load control module, an inverter in this case (col. 7, ll. 40-64).
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to implement into the device of Nakamura et al a PN detector and corrector, respectively, that provides the advantage of regulating the DC voltage applied to the inverter, as taught by Gilbreth et al.
- With respect to claim 4, Gilbreth et al disclose the PN correction factor having an lower limit value (col. 7, ll. 56-64, where the lower limit is when the signal at #212 is at least equal to the signal set at #216).
- With respect to claim 5, the PN voltage corrector increases the PN voltage correction factor in proportion to the DC voltage detection value when the DC voltage detection value is larger than the DC voltage reference value (col. 7, ll. 55-60; signal #218 increases when #212 is greater than #216).

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaji et al, Nakamura et al in view of Morimoto et al, and Nakamura et al in view of Gilbreth et al, separately, as applied to claim 1 above.

- With respect to claim 7, the above-mentioned references do not disclose the values of the reactor and capacitor chosen so that a resonant frequency is larger than 40 times the AC power supply frequency.
- The Examiner takes Official Notice for this limitation. Typically, the AC power supply is 60 Hz, which would make 40 times that frequency 2.4kHz. It would have been obvious to one having ordinary skill in the art at the time of the invention to make the reactor and capacitor values so that the resonant frequency is at least 40 times 60 Hz, or a value that is at least greater than 2.4kHz. One reason to make the resonant frequency at least 40 times greater than the power supply frequency is to generate less noise because the resonant frequency is significantly higher than the AC power supply frequency. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to select values for the reactor and capacitor, in the above-mentioned references, so that their resonant frequency is at least 40 times greater than the AC power supply frequency, thereby providing the advantage of generating less noise.
- With respect to claim 8, the above-mentioned references do not disclose the value of the capacitor chosen so that a maximum value of the DC voltage is made smaller than the rated voltage for the capacitor.
- The Examiner takes Official Notice for this limitation. It would have been obvious to one having ordinary skill in the art at the time of the invention to select

a capacitor value that it can handle the maximum DC voltage value. The motivation to do so is so the capacitor will not be damaged, even when the maximum DC voltage value is present. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to select a capacitor value, for the above-mentioned references, that can withstand the maximum DC voltage value, thereby providing the advantage of preventing the capacitor from being damaged.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaji et al, Nakamura et al in view of Morimoto et al, and Nakamura et al in view of Gilbreth et al, separately, as applied to claim 1 above, and further in view of Smith (5,561,595).

- Kawaji et al, Nakamura et al in view of Morimoto et al, and Nakamura et al in view of Gilbreth et al, separately, do not disclose a carrier frequency of the inverter selected to satisfy a predetermined AC power supply factor.
- Smith discloses selecting an inverter carrier frequency based on the input power factor of an AC input rectifier. The motivation to implement this feature is to correct the input power factor to near unity (abstract).
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to choose a carrier frequency of the inverter so as to control the input power factor, thereby providing the advantage of correcting the input power factor to near unity, as taught by Smith.

Allowable Subject Matter

10. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

    - With respect to claim 3, the Prior Art does not disclose dividing the DC reference voltage by the DC voltage detection value to get the PN voltage correction factor, and wherein the PN voltage corrector sets a predetermined maximum value of the PN voltage correction factor as the PN voltage correction factor when the DC voltage detection value is zero or less.

11. With respect to claims 2 and 6, the Prior Art does not disclose the limitations therein (including the base claim). However, note that this claim is provisionally rejected under Double Patenting. See rejection above.

Prior Art

12. Toda et al (6,002,218) disclose a compressor that can be driven by either a brushless motor or an induction motor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick Miller whose telephone number is 571-272-2070. The examiner can normally be reached on M-F, 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Martin can be reached on 571-272-2800 ext 41. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patrick Miller
Examiner
Art Unit 2837

pm
February 21, 2005

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